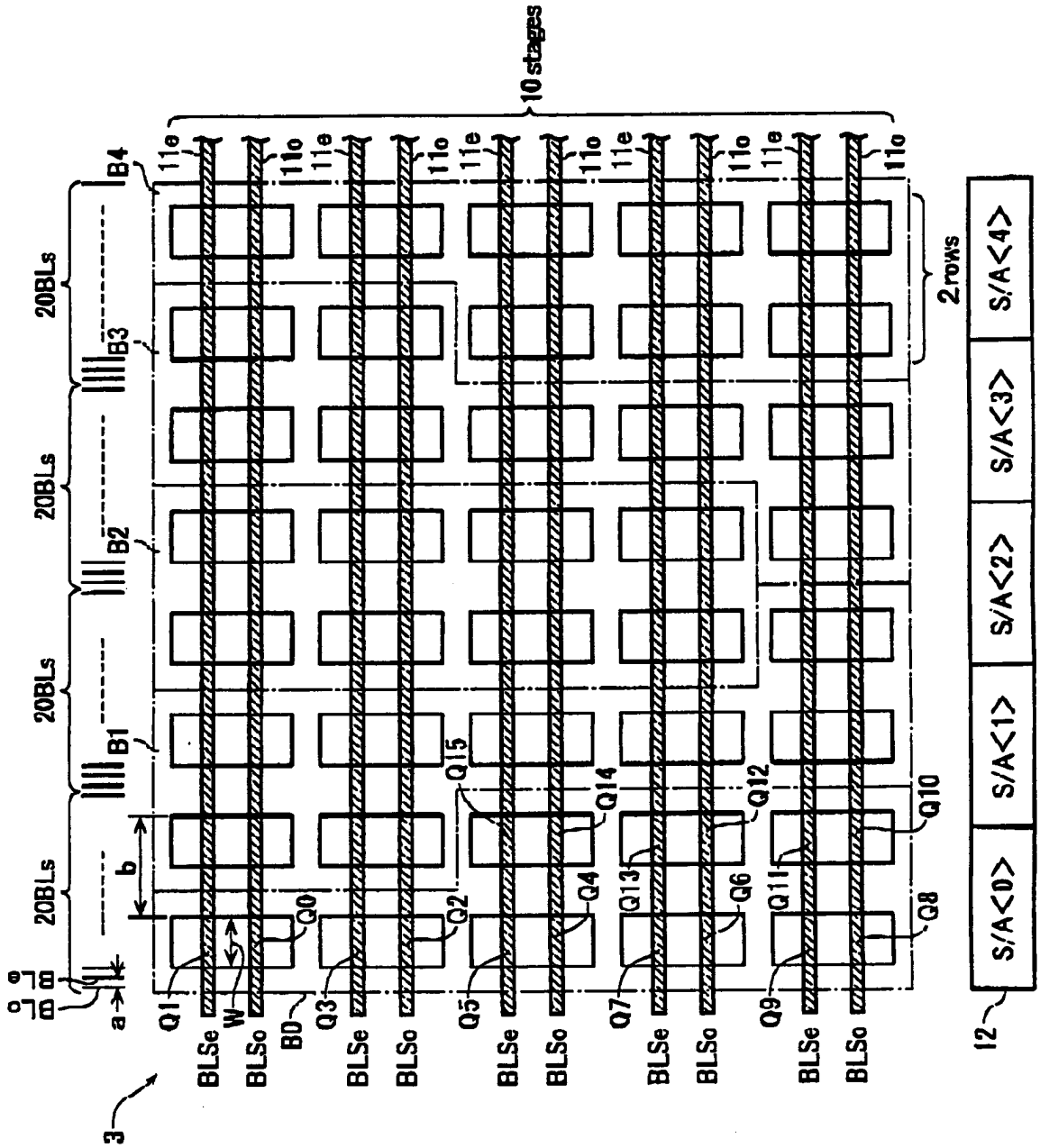

10 stages
2 rows
20BLs
B1
B2
B3
B4
BLo
BLe
a
b
W
S
BD
BLSe
BLSo
11e
11o
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
S/A<0>
S/A<1>
S/A<2>
S/A<3>
S/A<4>
3
12

FIG. 1

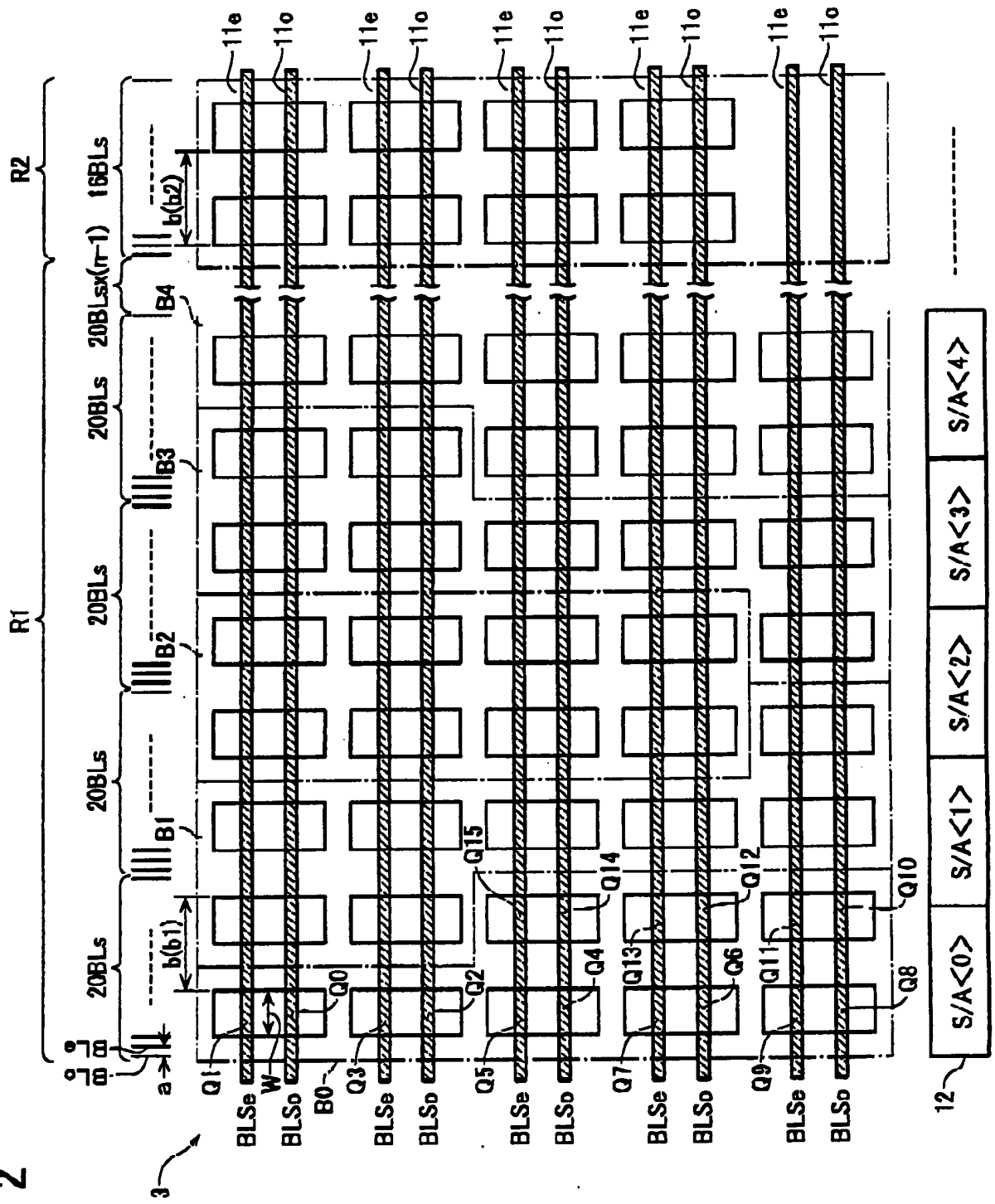

R1
R2
20BLs
20BLs×(n-1)
16BLs
B0
B1
B2
B3
B4
11e
11o
b(b1)
b(b2)
a
W
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
BLSe
BLSo
3
12
S/A<0>
S/A<1>
S/A<2>
S/A<3>
S/A<4>

FIG. 2

FIG. 3

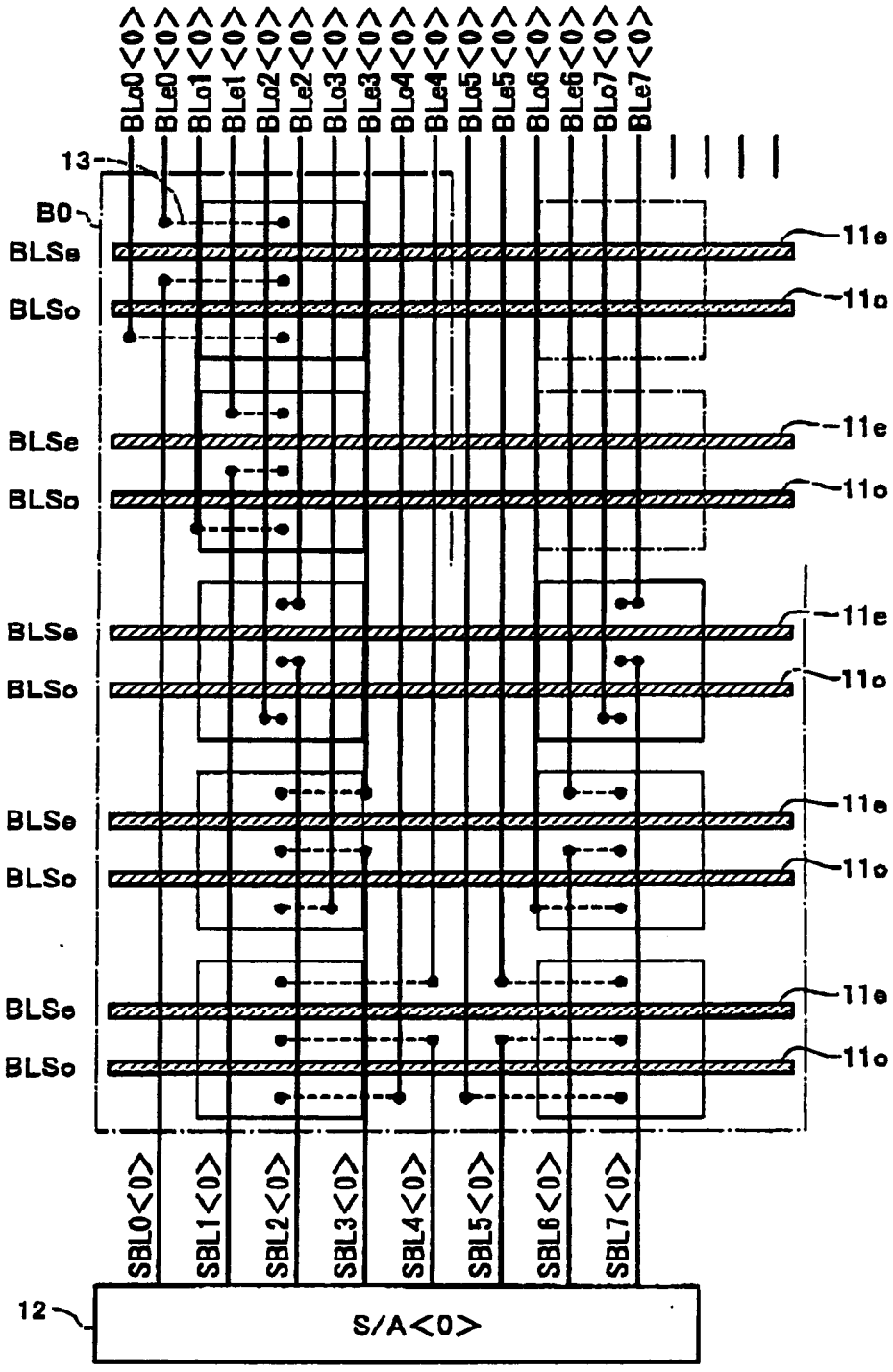

BLo0<0>
BLe0<0>
BLo1<0>
BLe1<0>
BLo2<0>
BLe2<0>
BLo3<0>
BLe3<0>
BLo4<0>
BLe4<0>
BLo5<0>
BLe5<0>
BLo6<0>
BLe6<0>
BLo7<0>
BLe7<0>
13
B0
BLSe
BLSo
11e
11o
SBL0<0>
SBL1<0>
SBL2<0>
SBL3<0>
SBL4<0>
SBL5<0>
SBL6<0>
SBL7<0>
12
S/A<0>

FIG. 4

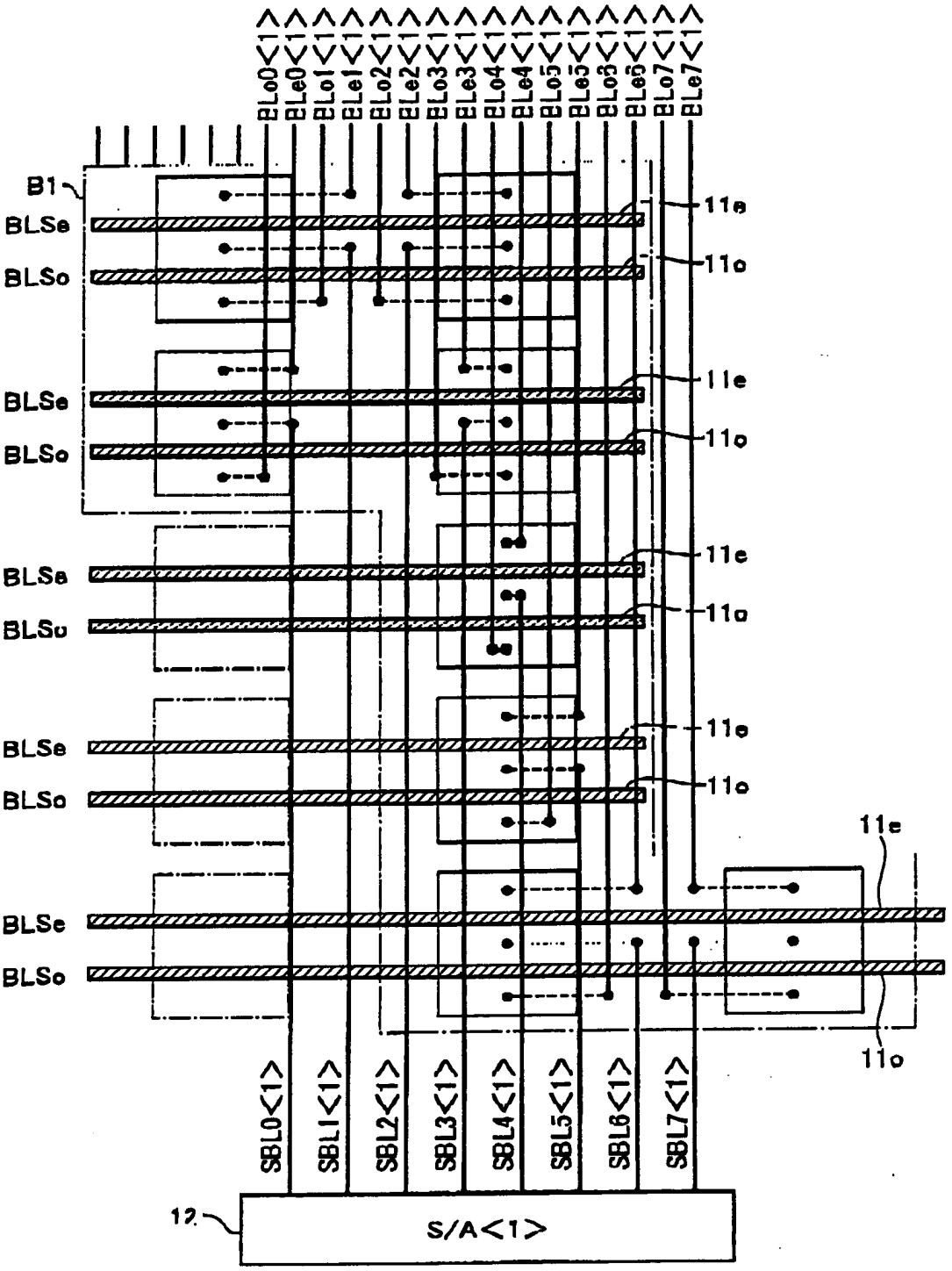

BLo0<1>
BLe0<1>
BLo1<1>
BLe1<1>
BLo2<1>
BLe2<1>
BLo3<1>
BLe3<1>
BLo4<1>
BLe4<1>
BLo5<1>
BLe5<1>
BLo6<1>
BLe6<1>
BLo7<1>
BLe7<1>
B1
BLSe
BLSo
11e
11o
SBL0<1>
SBL1<1>
SBL2<1>
SBL3<1>
SBL4<1>
SBL5<1>
SBL6<1>
SBL7<1>
12
S/A<1>

FIG. 5

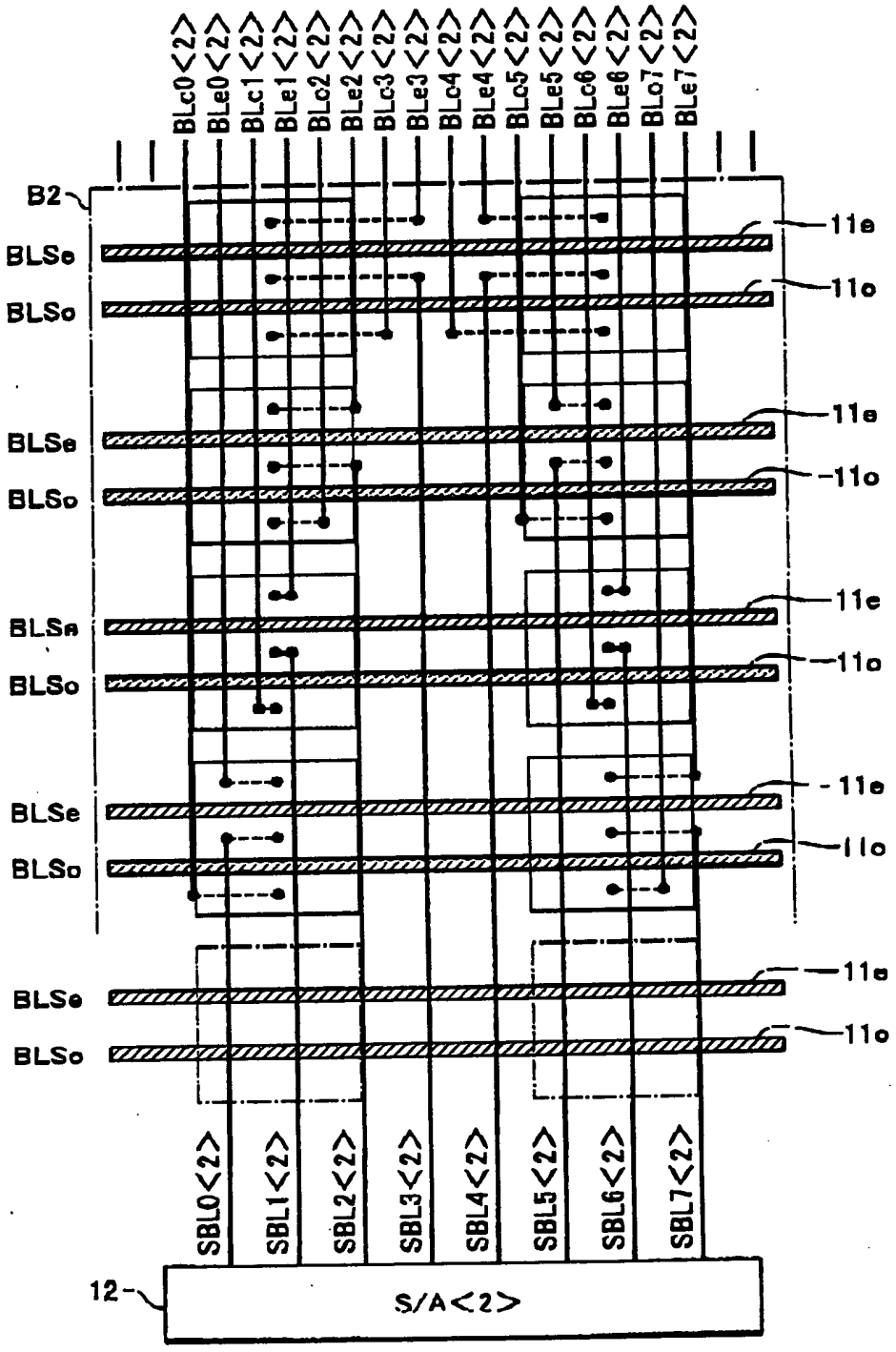

BLc0<2>
BLe0<2>
BLc1<2>
BLe1<2>
BLc2<2>
BLe2<2>
BLc3<2>
BLe3<2>
BLc4<2>
BLe4<2>
BLc5<2>
BLe5<2>
BLc6<2>
BLe6<2>
BLc7<2>
BLe7<2>
B2
BLSe
BLSo
11e
11o
SBL0<2>
SBL1<2>
SBL2<2>
SBL3<2>
SBL4<2>
SBL5<2>
SBL6<2>
SBL7<2>
12
S/A<2>

FIG. 6

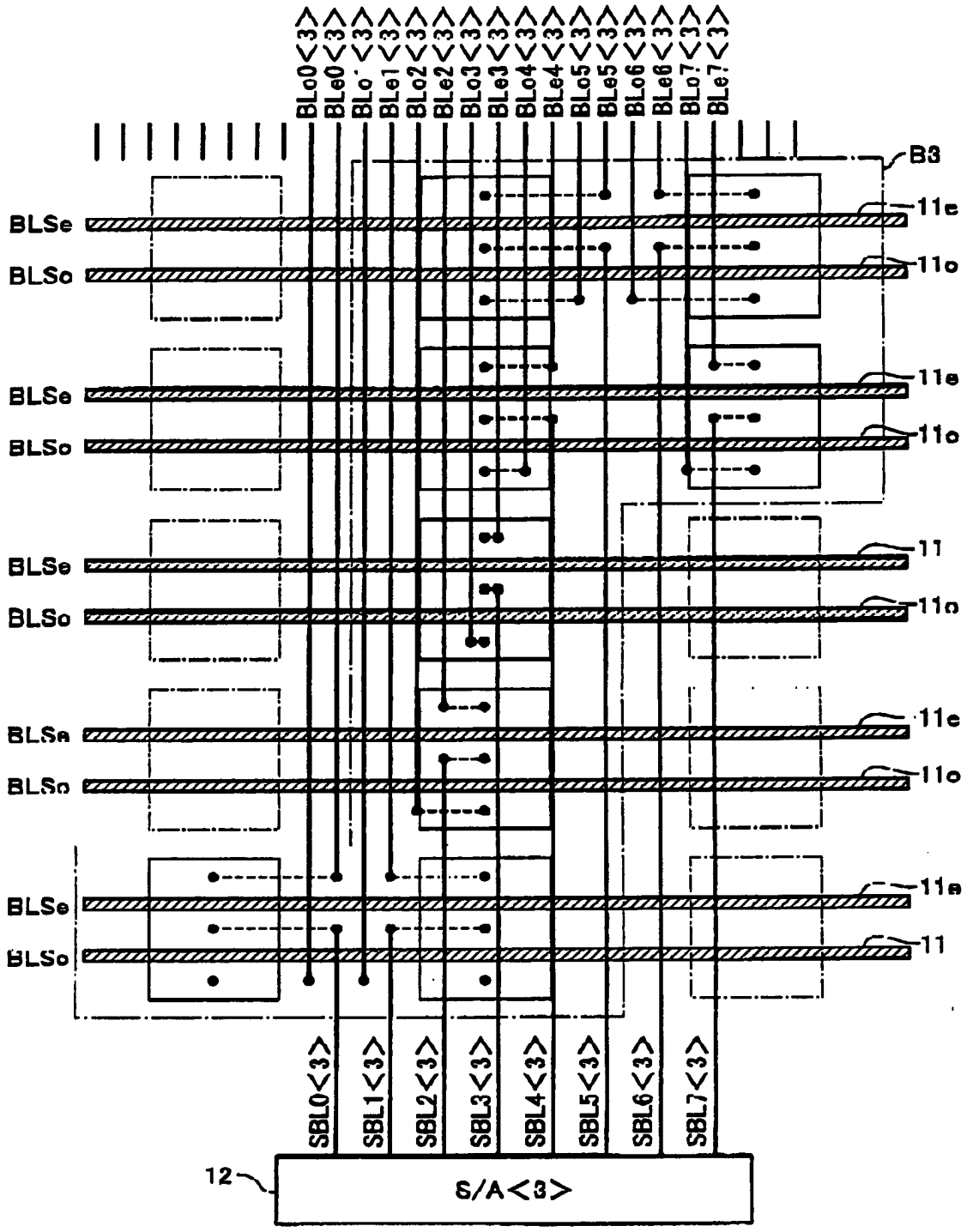
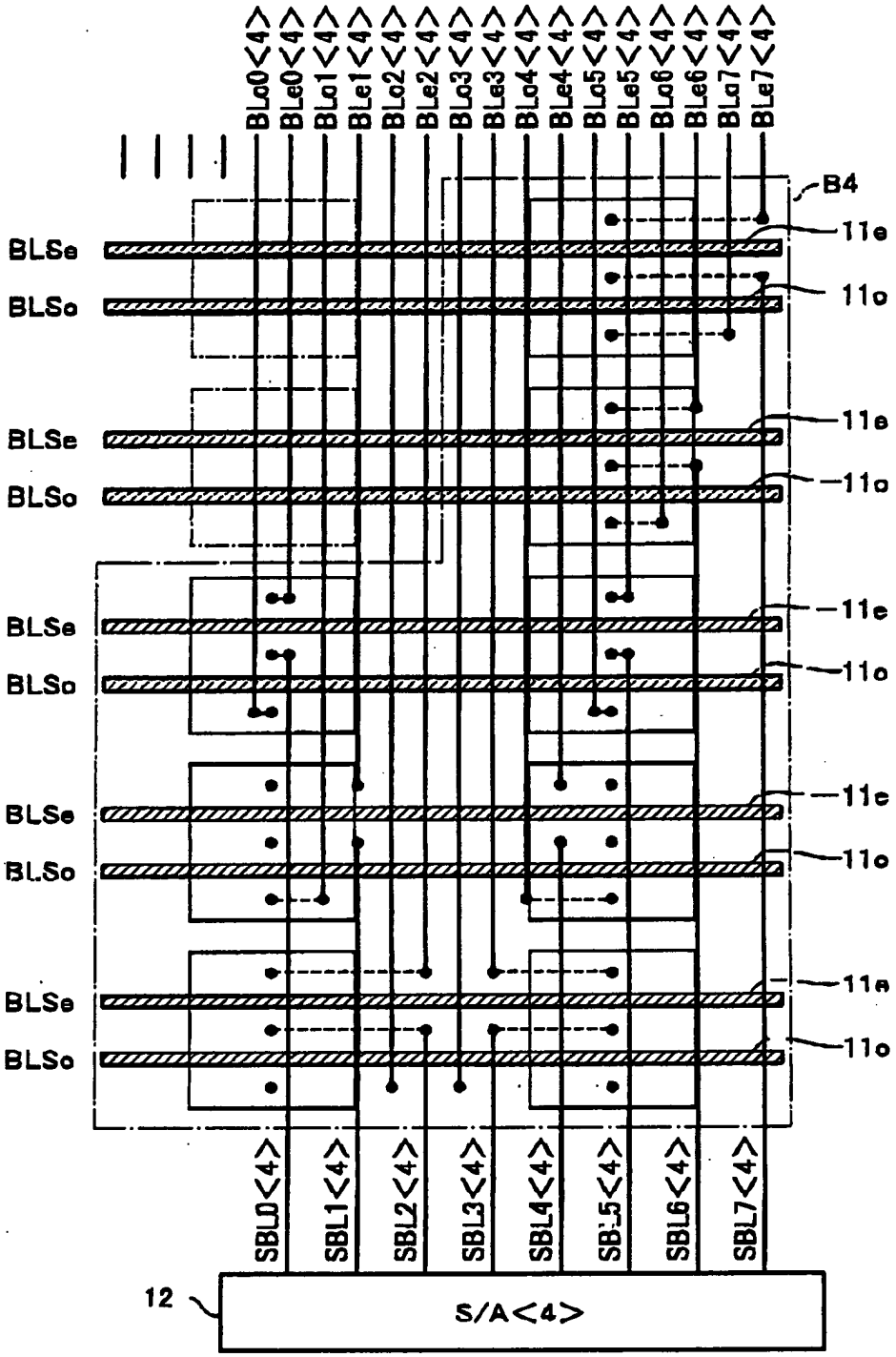

BLo0<3>
BLe0<3>
BLo1<3>
BLe1<3>
BLo2<3>
BLe2<3>
BLo3<3>
BLe3<3>
BLo4<3>
BLe4<3>
BLo5<3>
BLe5<3>
BLo6<3>
BLe6<3>
BLo7<3>
BLe7<3>
B3
BLSe
BLSo
11e
11o
11
SBL0<3>
SBL1<3>
SBL2<3>
SBL3<3>
SBL4<3>
SBL5<3>
SBL6<3>
SBL7<3>
12
S/A<3>

FIG. 7


BLo0<4>
BLe0<4>
BLo1<4>
BLe1<4>
BLo2<4>
BLe2<4>
BLo3<4>
BLe3<4>
BLo4<4>
BLe4<4>
BLo5<4>
BLe5<4>
BLo6<4>
BLe6<4>
BLo7<4>
BLe7<4>
B4
BLSe
BLSo
11e
11o
SBL0<4>
SBL1<4>
SBL2<4>
SBL3<4>
SBL4<4>
SBL5<4>
SBL6<4>
SBL7<4>
12
S/A<4>

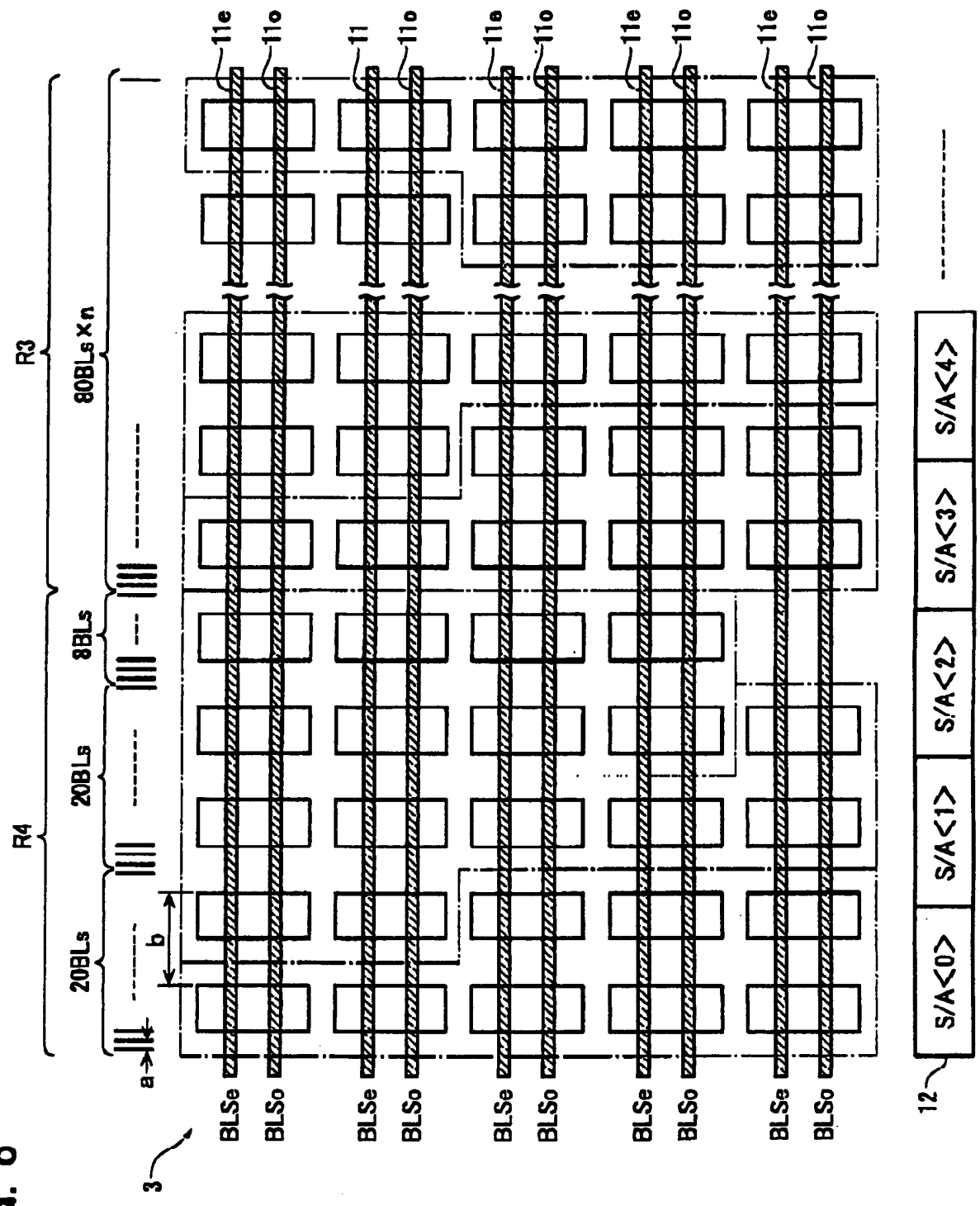

11e
11o
11
R3
80BLs x n
8BLs
20BLs
R4
20BLs
b
a
3
BLSe
BLSo
S/A<0>
S/A<1>
S/A<2>
S/A<3>
S/A<4>
12

FIG. 8

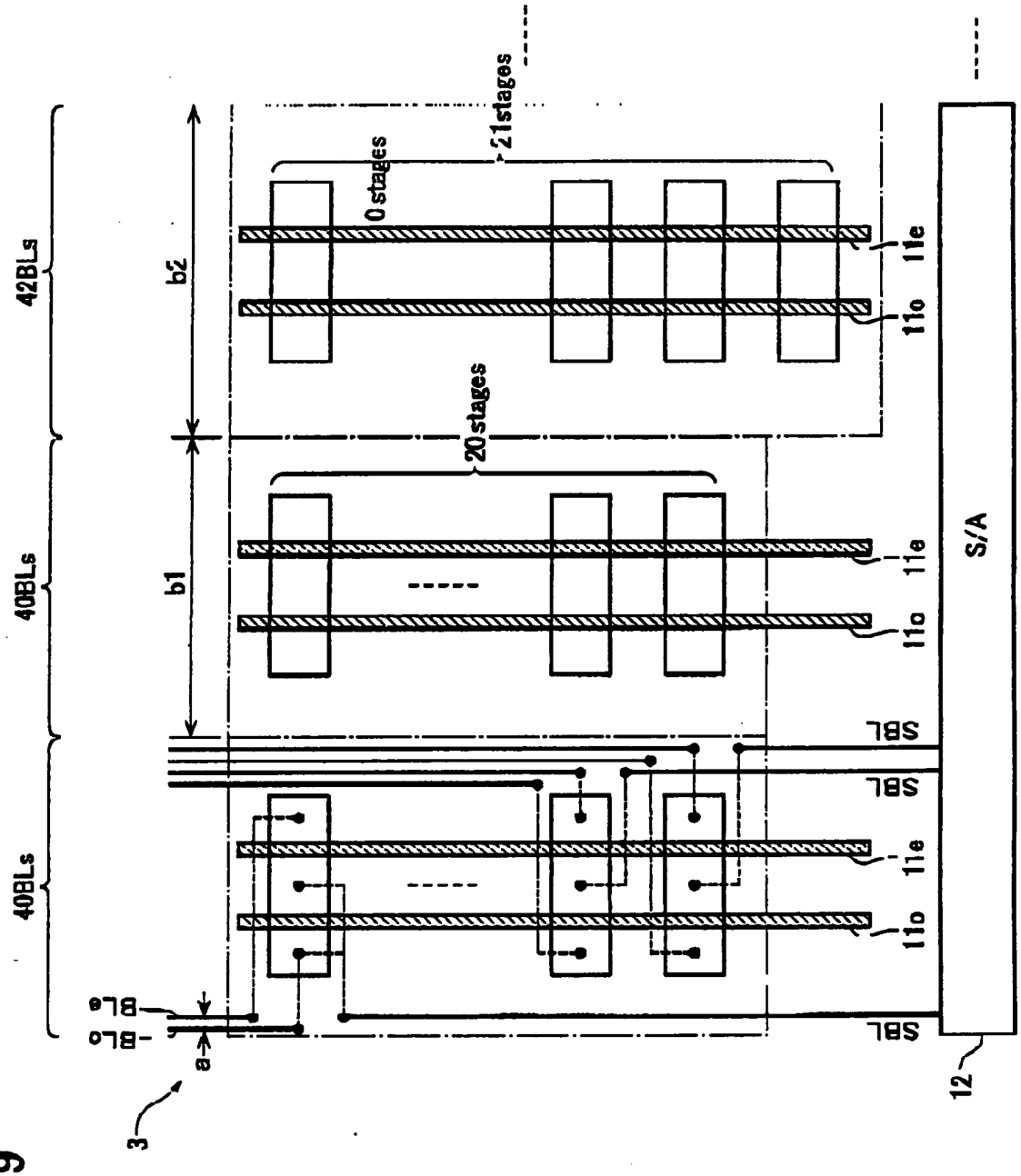

42BLs
40BLs
40BLs
b2
b1
21stages
0 stages
20 stages
11e
11o
S/A
SBL
BLe
BLo
a
3
12

FIG. 9

FIG. 10

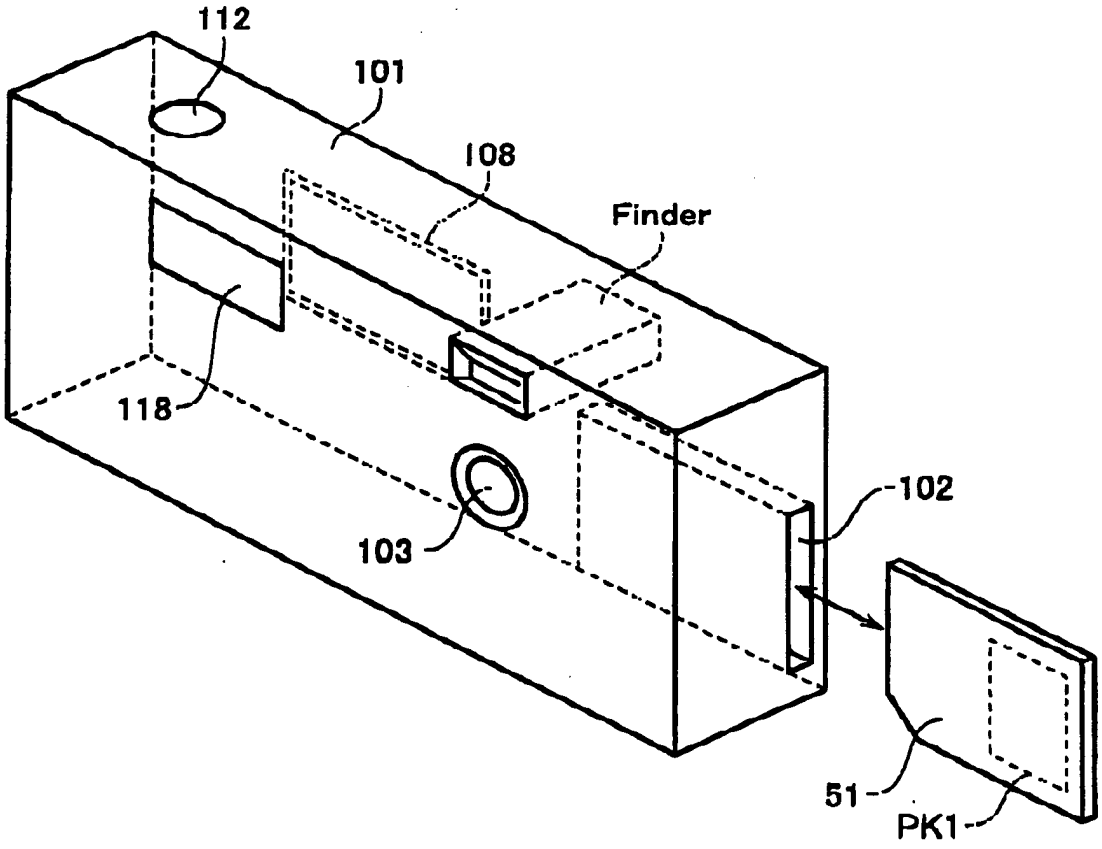


FIG. 11

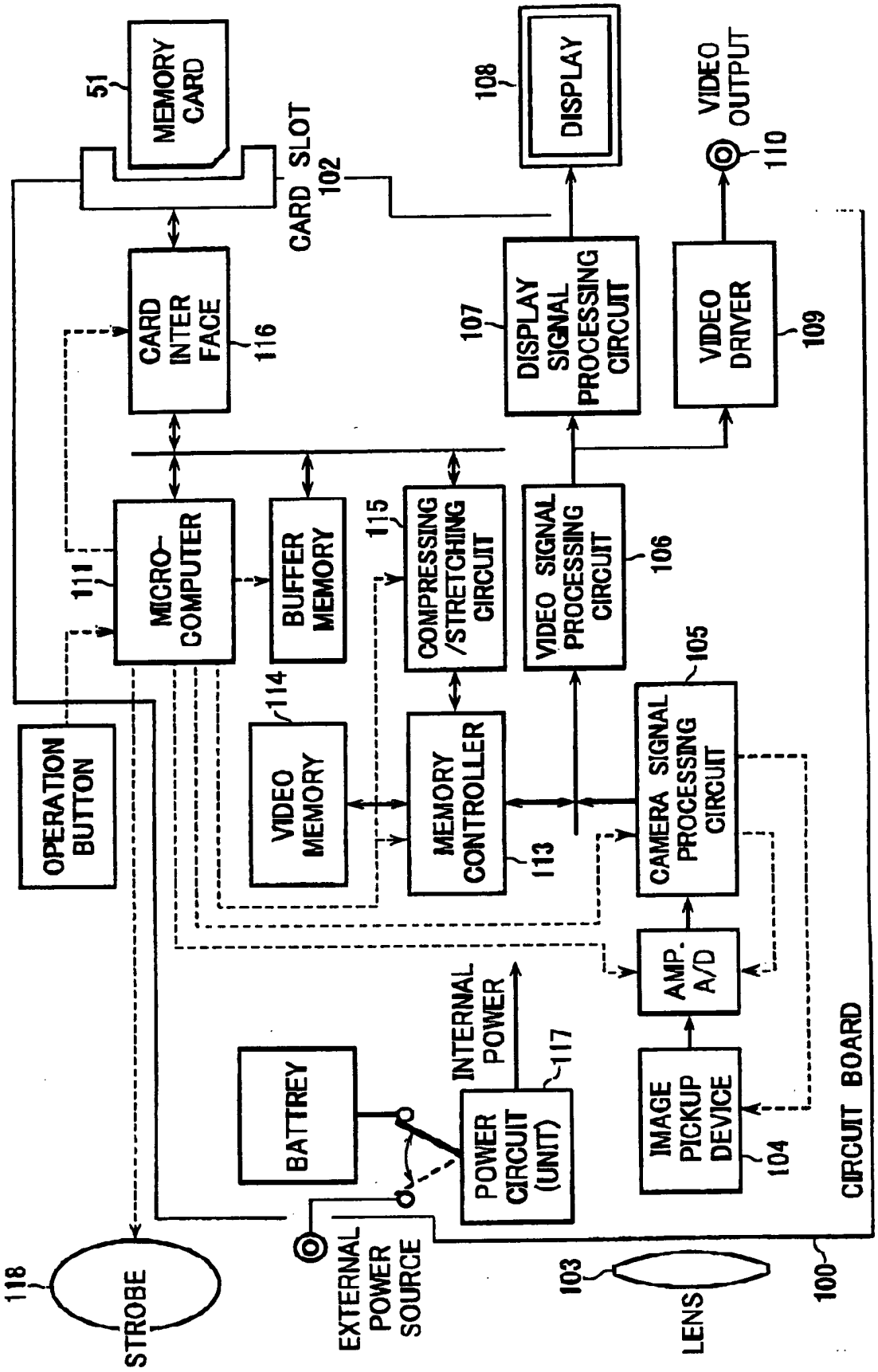

MEMORY CARD
51
CARD SLOT
102
DISPLAY
108
VIDEO OUTPUT
110
CARD INTER FACE
116
DISPLAY SIGNAL PROCESSING CIRCUIT
107
VIDEO DRIVER
109
MICRO-COMPUTER
111
BUFFER MEMORY
115
COMPRESSING /STRETCHING CIRCUIT
VIDEO SIGNAL PROCESSING CIRCUIT
106
OPERATION BUTTON
VIDEO MEMORY
114
MEMORY CONTROLLER
113
CAMERA SIGNAL PROCESSING CIRCUIT
105
AMP. A/D
INTERNAL POWER
117
BATTREY
POWER CIRCUIT (UNIT)
IMAGE PICKUP DEVICE
104
CIRCUIT BOARD
118
STROBE
EXTERNAL POWER SOURCE
103
LENS
100

FIG. 12A

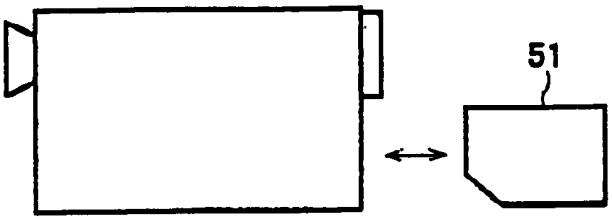


FIG. 12B

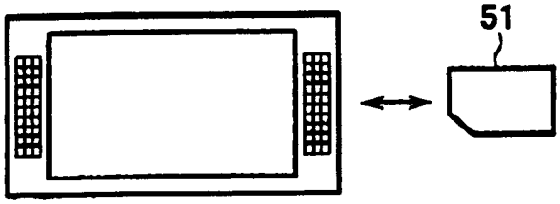


FIG. 12C

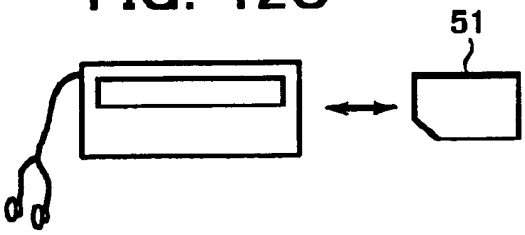


FIG. 12D

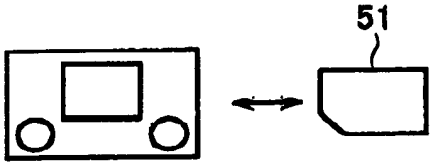


FIG. 12E

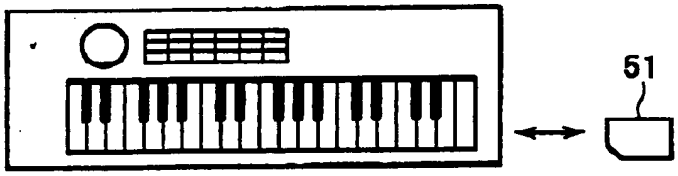


FIG. 12F

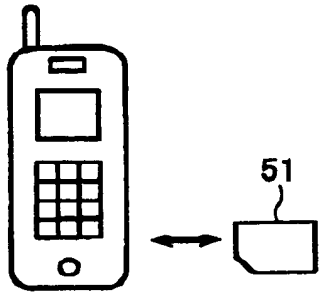


FIG. 12G

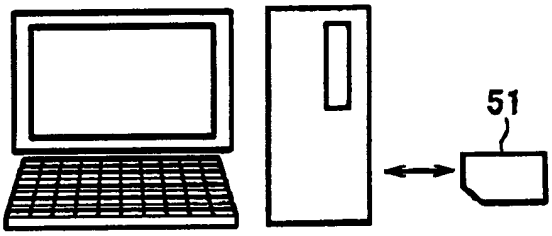


FIG. 12H

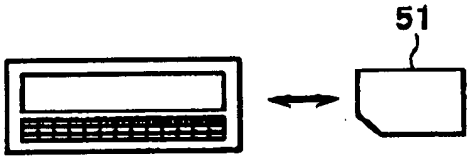


FIG. 12I

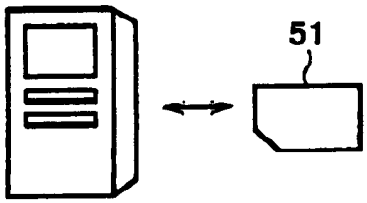


FIG. 12J

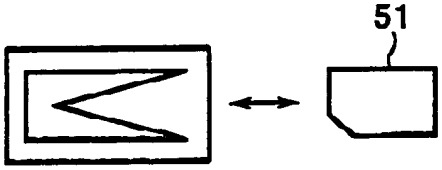


FIG. 13

Prior art

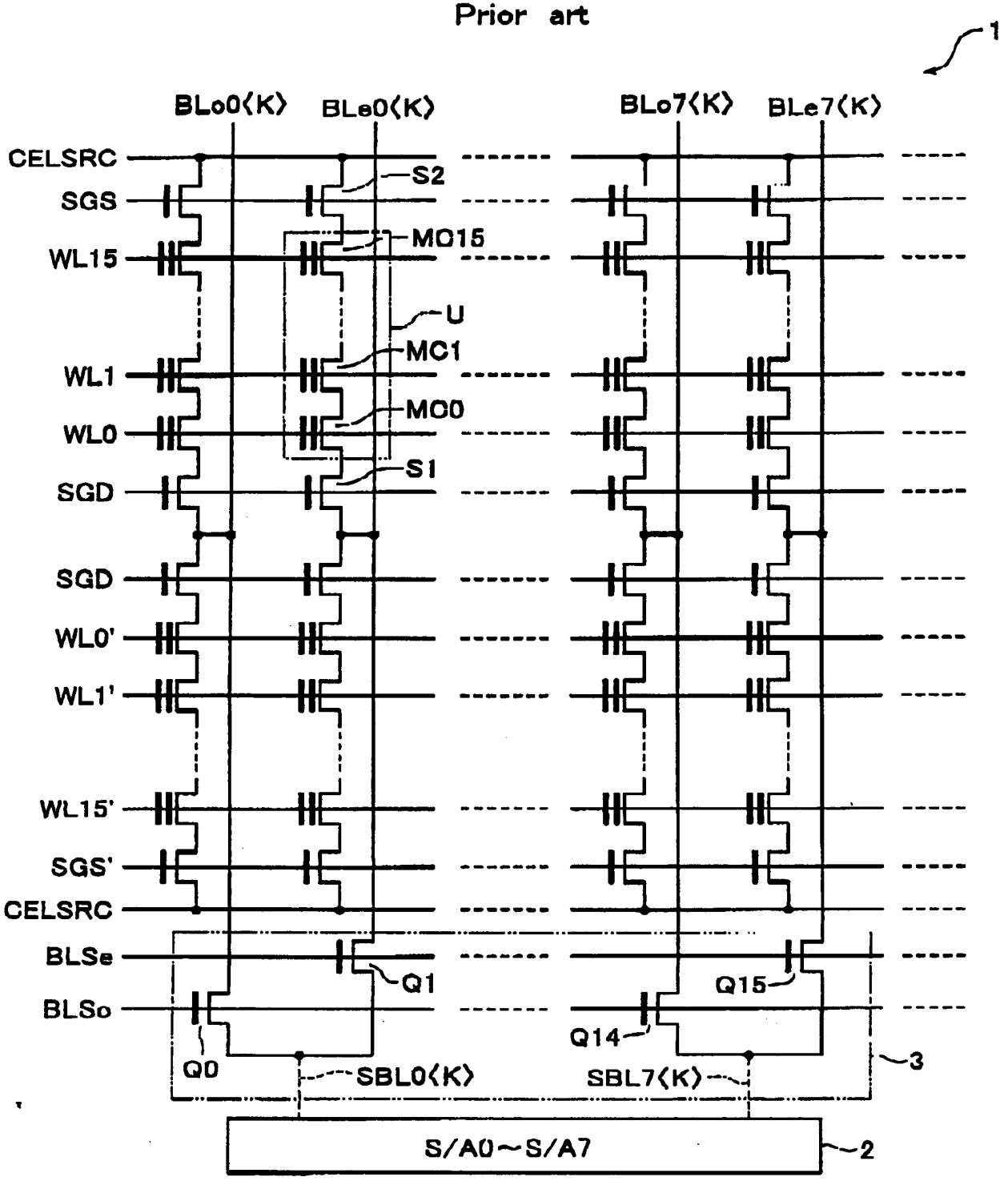
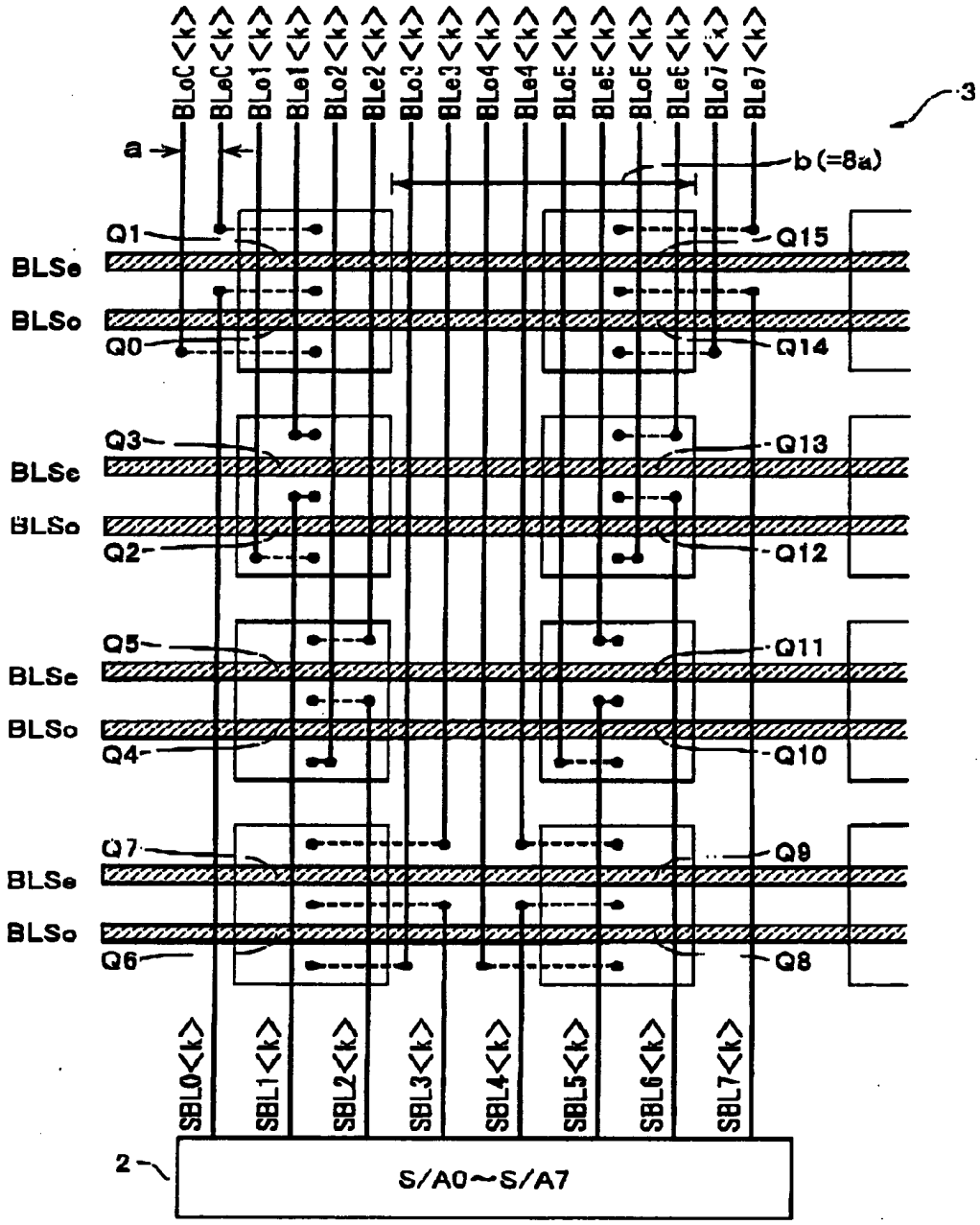


FIG. 14


BLoC<k>
BLeC<k>
BLo1<k>
BLe1<k>
BLo2<k>
BLe2<k>
BLo3<k>
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BLe4<k>
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BLeE<k>
BLoE<k>
BLeE<k>
BLo7<k>
BLe7<k>
3
a
b (=8a)
Q1
Q15
BLSe
BLSo
Q0
Q14
Q3
Q13
BLSe
BLSo
Q2
Q12
Q5
Q11
BLSe
BLSo
Q4
Q10
Q7
Q9
BLSe
BLSo
Q6
Q8
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SBL6<k>
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2
S/A0~S/A7